ABSTRACT OF THE DISCLOSURE

Provided is a semiconductor memory device having an output driver for high frequency operation. In the output driver of the semiconductor memory device, a first NMOS transistor and a second NMOS transistor are connected in series, the drain of the first NMOS transistor is connected to an output pad, and the source of the second NMOS transistor is connected to a ground voltage. In addition, a first internal voltage is applied to the gate of the first NMOS transistor, a second internal voltage is applied to a gate of the second NMOS transistor, and a voltage level of the second internal voltage is lower than the voltage level of an external supply voltage. The second internal voltage is generated directly from an internal voltage generating circuit of the semiconductor memory device or is externally applied. The voltage level of the second internal voltage is different from the level of an operating voltage of the semiconductor memory device.

J:\SAM\0464\464patapp2.doc